REMARKS

Reconsideration of the application is requested.

Claims 1-10 are now in the application. Claims 1-10 are subject to examination. Claims 1, 8, and 9 have been amended. Claim 10 has been added.

Applicant appreciates the indication that claim 9 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."

In response to the indication of allowability, claim 9 has been rewritten in independent form including all of the limitations of claims 1 and 8.

On page 2 of the above-identified Office Action, claims 1-9 have been rejected as being obvious over U.S. Patent No. 6,163,837 to Chan et al. in view of U.S. Patent No. 6,609,193 B1 to Douglas et al. under 35 U.S.C. § 103. Applicant respectfully traverses.

In *KSR Int'l Co. v. Teleflex, Inc.,* No 04-1350 (U.S. Apr. 30,2007), the court reaffirmed the *Graham* factors in the determination of obviousness under *35 U.S.C.* § 103(a).

MPEP 2141 Section II sets forth the Graham Factual Inquiries that are used to determine obviousness under 35 U.S.C. 103. This section is copied below:

> II. BASIC CONSIDERATIONS WHICH APPLY TO OBVIOUSNESS REJECTIONS
>
> When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to:
>
> (A) The claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined.

In KSR, the Court noted that the analysis supporting a rejection under 35 U.S.C. § 103(a) should be made explicit, and that it was "important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements"; in the manner claimed. The Court specifically stated:

Often, it will be necessary...to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an **apparent** reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis **should be made explicit**.

When one considers the teachings in Douglas et al. and Chan et al. **as a whole**, and **without the benefit of impermissible hindsight vision** afforded by the claimed invention, they do not suggest the desirability and thus the obviousness of making the invention defined by claim 1.

Claim 1 specifies that the pipeline instructions are instructing said program-controlled unit to stop an individual one of said plurality of pipeline stages, more than one of said plurality of pipeline stages, or all of said plurality of pipeline stages without creating any conditions for which one pipeline stage, a plurality pipeline stages, or all pipeline stages are stopped.

Douglas et al. teach using hardware to evaluate whether certain conditions, which exist in the pipeline stages, necessitate stalling the pipe stages. This is something very different from providing pipeline instructions that instruct the program-controlled unit to stop pipeline stages as specified in claim 1. Douglas

et al. do not teach or suggest pipeline instructions that instruct the program-controlled unit to stop pipeline stages.

The alleged instructions for stalling that are taught by Douglas et al. are hardware signals that are generated by the buffers 502A, 502B of the instruction decode pipeline 400', when a buffer 502A, 502B becomes full (column 6, lines 62-67, column 7, lines 54-62, and Fig. 5). It is these stall signals, which are generated by the buffers 502A, 502B, that are evaluated by further control logic 401 to turn off the clock to a pipestage (column 11, lines 15-16 and column 6, lines 65-67).

Chan et al teach nothing related to overfilled buffers, but rather simply teach inserting a NOP instruction into code when there is a long latency instruction (column 7, lines 45-54).

One of ordinary skill in the art considering the teachings of Douglas et al. and Chan et al. might have obtained a suggestion to modify the teaching in Chan et al. by providing a buffer that generates a stall signal when the buffer is full and by additionally also inserting a NOP instruction into the code when there is a long latency instruction.

One of ordinary skill in the art considering the teachings of Douglas et al. and Chan et al., however, would not have obtained a suggestion to provide pipeline

instructions that instruct the program-controlled unit to stop pipeline stages. The invention as defined by claim 1 is not obvious.

Claim 8 specifies that during normal operation, said program-controlled unit is configured to block execution of the pipeline instructions, which instruct stopping.

With regard to claim 8, the Examiner stated that Douglas et al. is configured for blocking the execution of the instructions, which instruct stopping, and has referred to column 9, lines 50-58, column 10, lines 1-6, and column 13, lines 38-42 for support of that assertion.

The cited portion of Douglas et al. does not teach blocking the execution of instructions that instruct pipeline stages to stop. Douglas et al. teach two different types of processes: a blocking stall and a non-blocking stall. In a blocking stall, every pipestage in the instruction decode pipeline is stopped regardless of the thread ID or the validity of the instructions in the pipe. In a non-blocking stall, instructions with a certain thread ID are stalled, but the decoder continues to decode instructions with other thread ID's (column 9, line 50 through column 10, line 6).

In each case, a stalling signal is being executed- either a blocking stall or a non-blocking stall. In neither case is the execution of a stalling signal being blocked. The particular stalling signal is different in each case. In one case,

the stalling signal is generated to block instructions with every thread ID, whereas in the other case the stalling signal is generated to block instructions with only a certain thread ID.

No teaching can be found that is related to not executing a blocking stall or non-blocking stall.

Further, the instructions in the pipeline that will be stalled by the blocking stall or by the non-blocking stall, are not pipeline instructions that instruct the program-controlled unit to stop one or more pipeline stages.

Claim 10 has been added to even further distinguish the invention from the prior art. Claim 10 is somewhat patterned after claim 9, which has been indicated as being allowable. Support for claim 10 can be found by referring to the specification at page 10, line 19 through page 11, line 8.

Claim 10 specifies that said program-controlled unit is configured to execute the pipeline instructions in a testing and/or initialization mode of operation and to block execution of the pipeline instructions in a mode of operation in which said program-controlled unit is not being tested and/or initialized.

The prior art is silent regarding blocking execution of the pipeline instructions in a testing and/or initialization mode of operation and executing the pipeline instructions in another mode of operation. Also note that claim 1, from which

claim 10 depends, specifies that the claimed pipeline instructions instruct the program-controlled unit to stop one or more pipeline stages. Douglas et al. merely teach a stalling signal that is generated by a buffer when the buffer is full. Douglas et al. do not teach instructions that instruct stopping one or more pipestages (Also see the discussion provided above in regard to claim 8).

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 9. Claims 1 and 9 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-10 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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